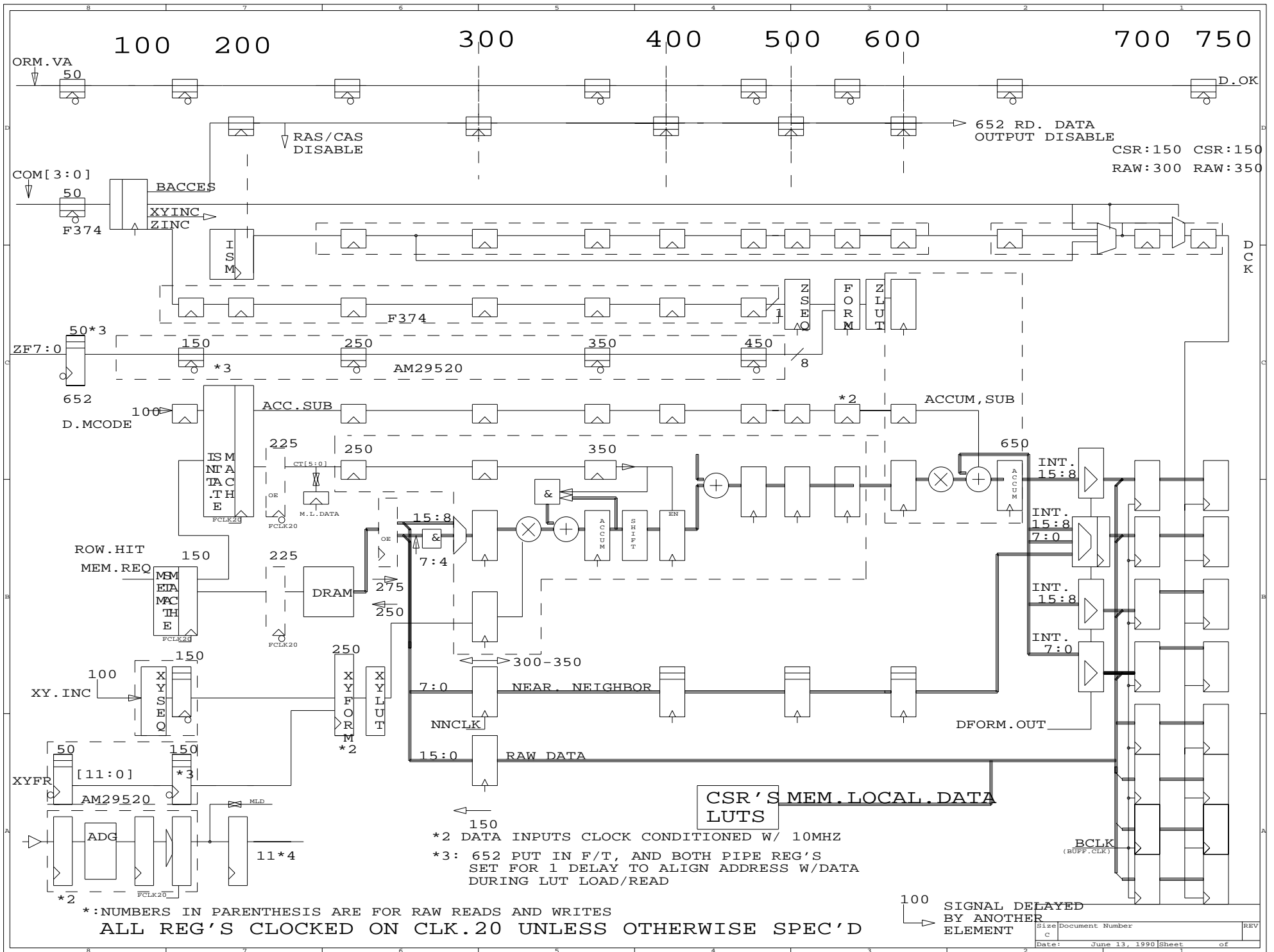
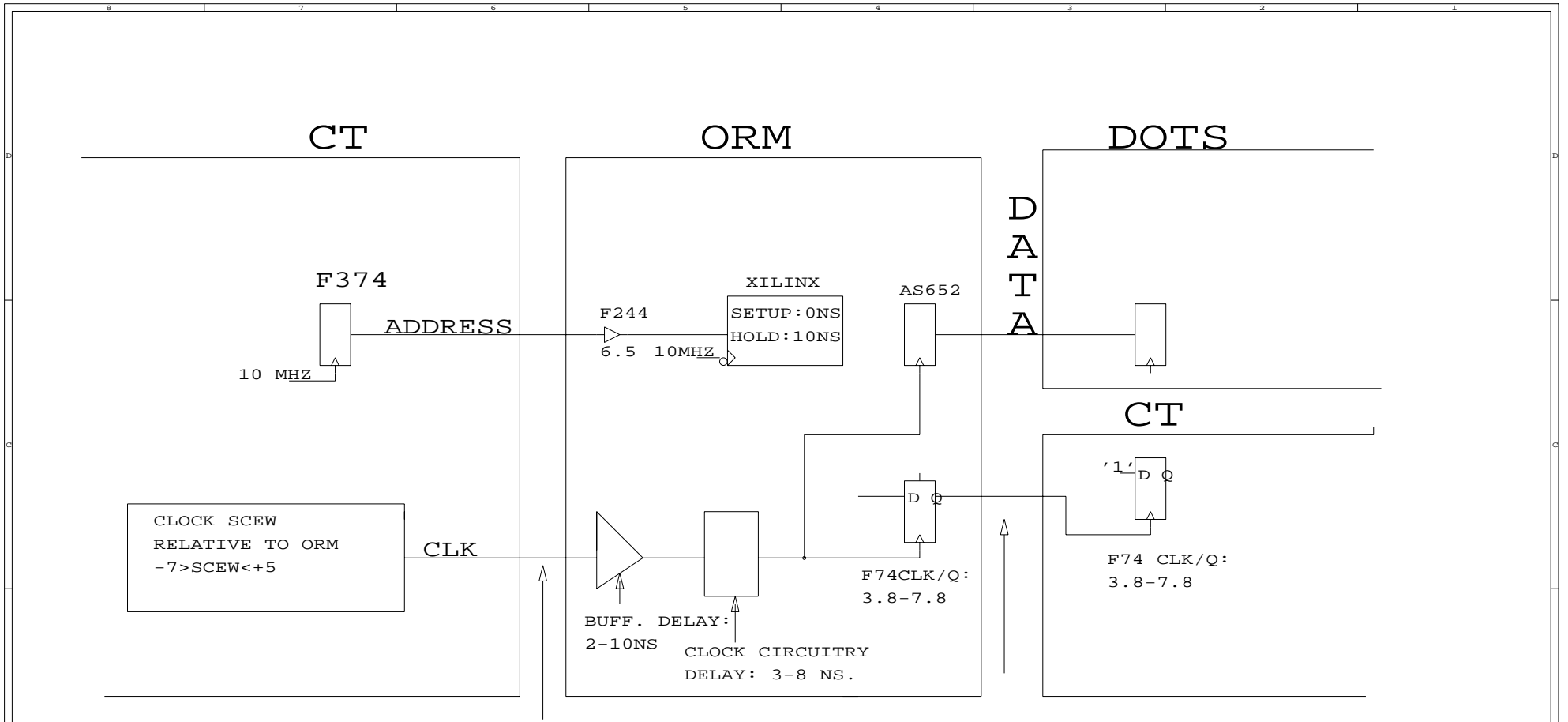


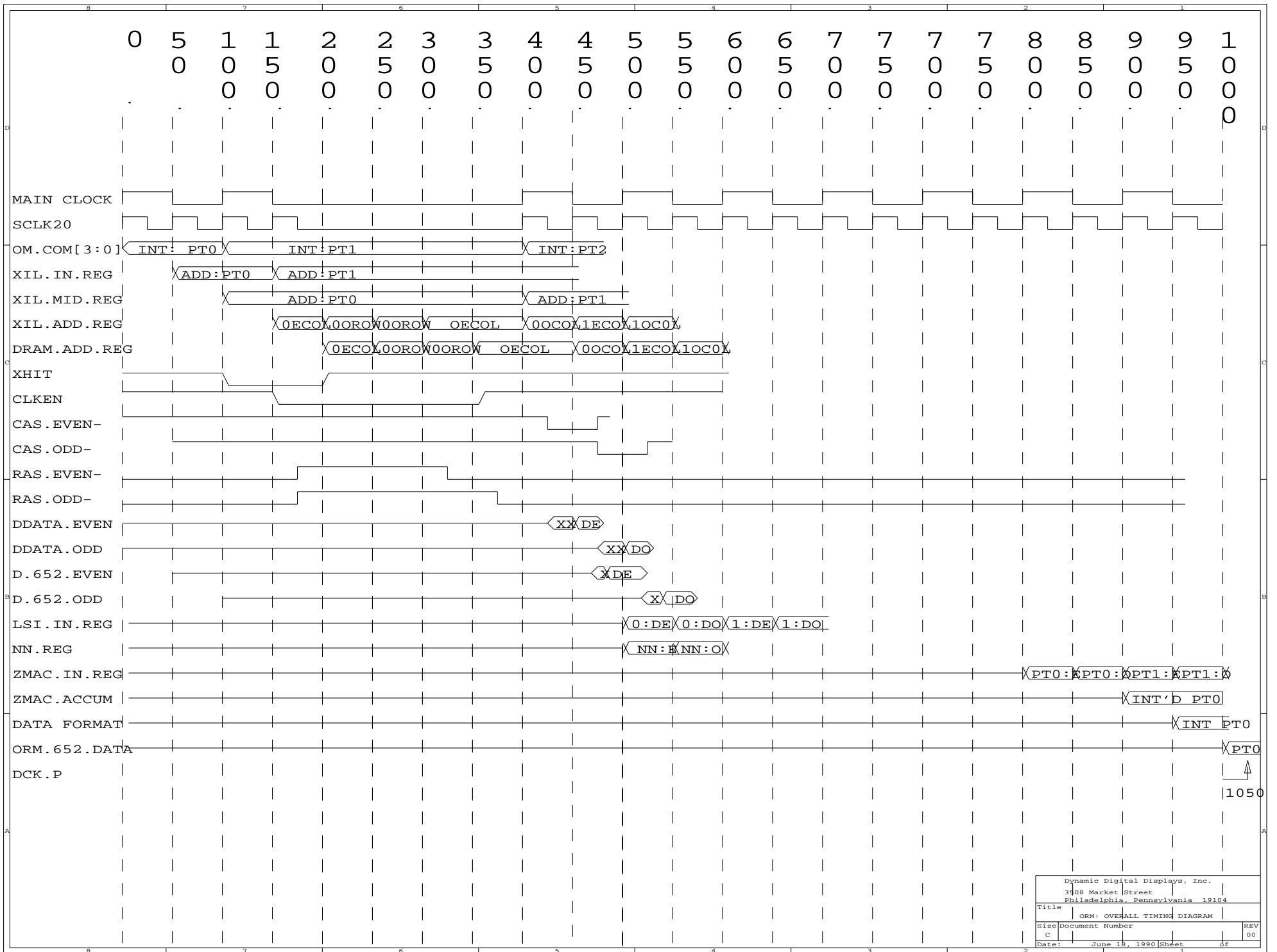
\*: USED FOR MIXED MODE, NON-RESAMPLING CONVOLUTIONS

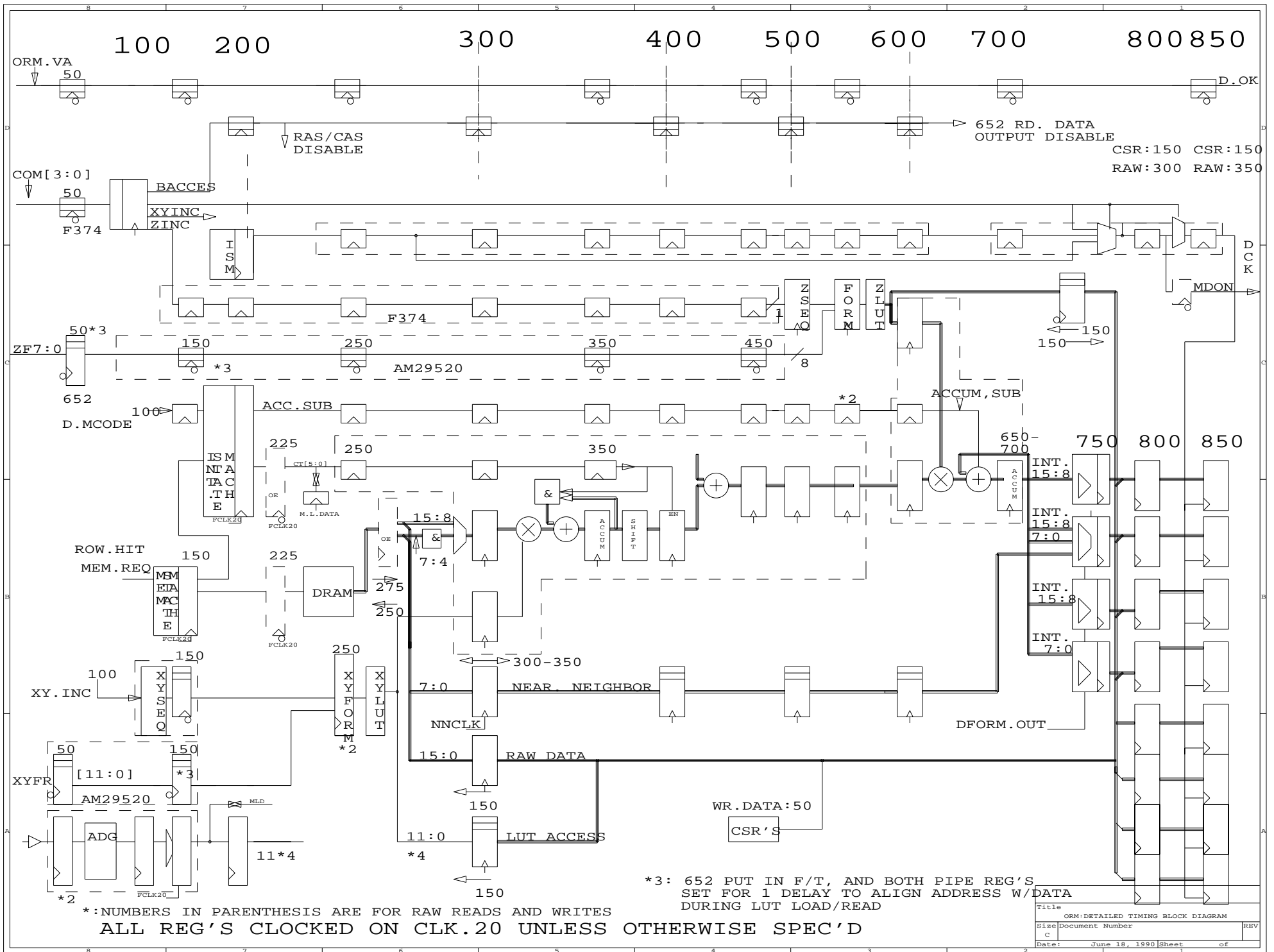




TRACE/CONN/BP.DELAY: 8 NS                      TRACE/CONN/BP.DELAY: 8 NS

MAX CLK/Q: DATA TO DOTS: 5+10+8+9+8: 40NS  
 MAX CLK/Q DELAY TO ORM: +5 +7.8+10 NS+6.5==29.3 nSEC  
 DCK: MAX CLK/Q: 54.6 NSEC

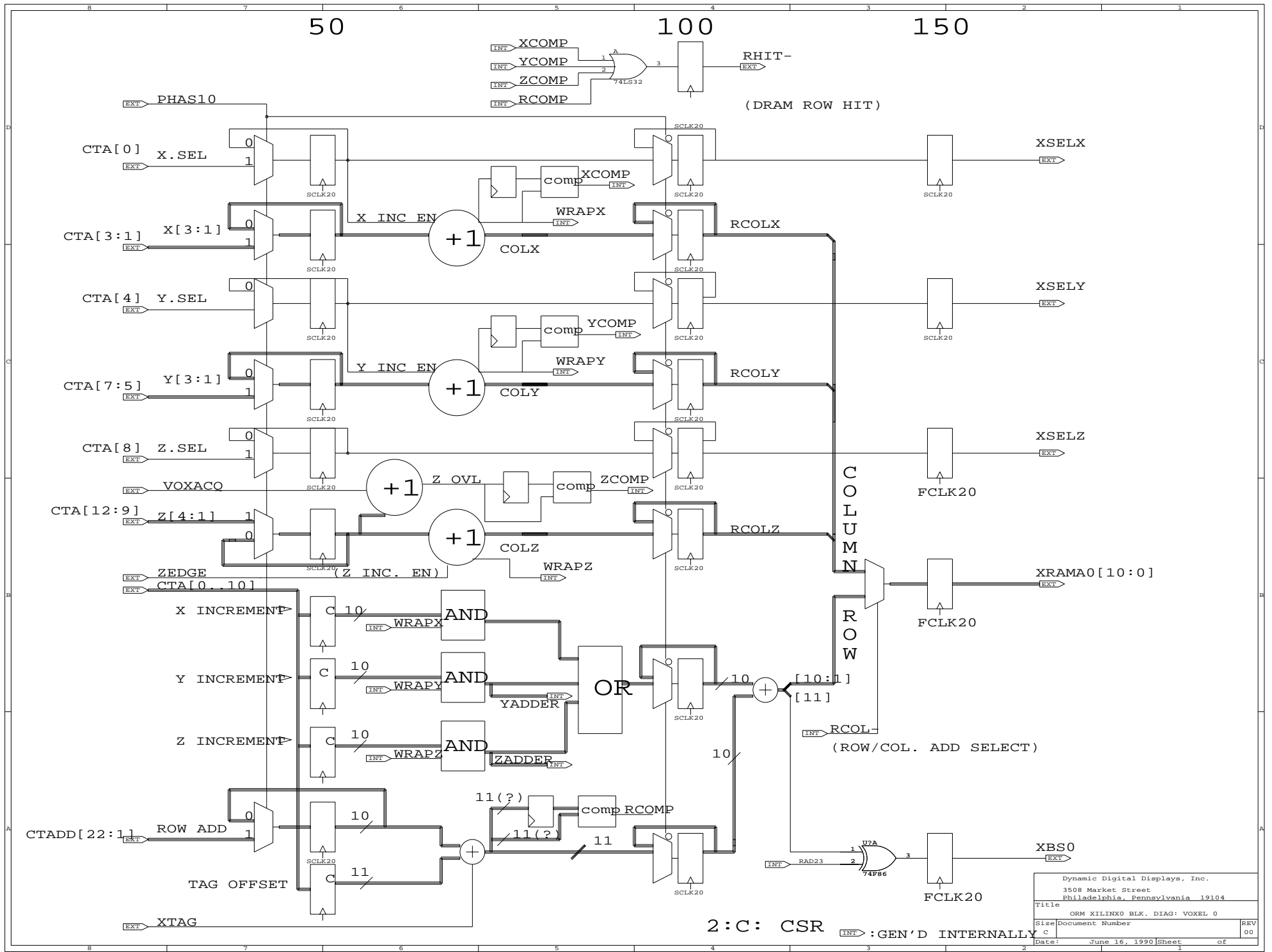




\*:NUMBERS IN PARENTHESIS ARE FOR RAW READS AND WRITES  
 ALL REG'S CLOCKED ON CLK.20 UNLESS OTHERWISE SPEC'D

\*3: 652 PUT IN F/T, AND BOTH PIPE REG'S  
 SET FOR 1 DELAY TO ALIGN ADDRESS W/DATA  
 DURING LUT LOAD/READ

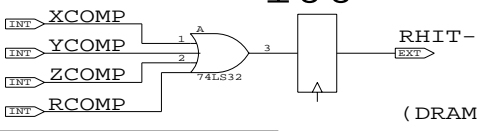
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Size	Document Number	REV
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Date:	June 18, 1990	Sheet 1 of 1



50

100

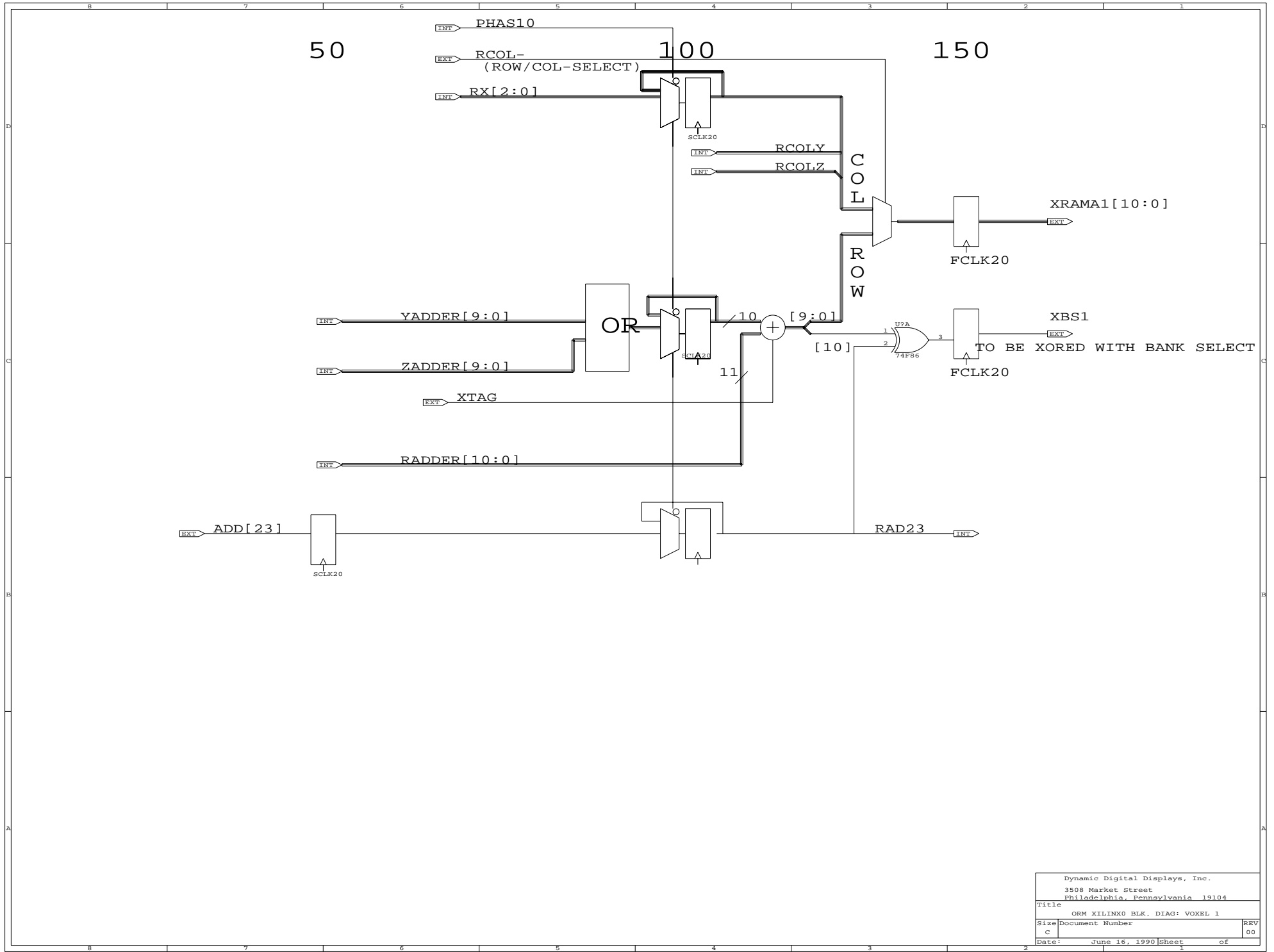
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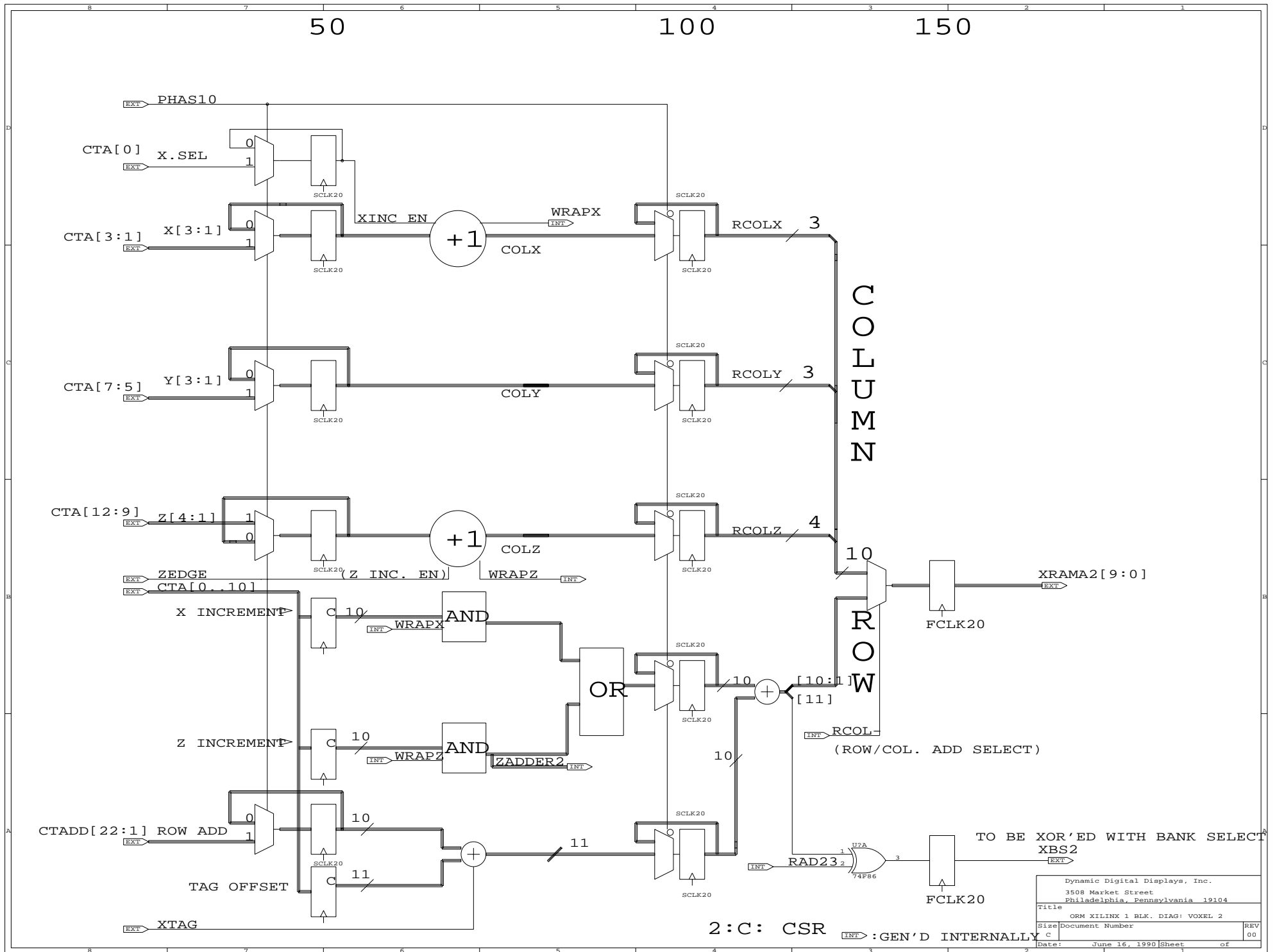


(DRAM ROW HIT)

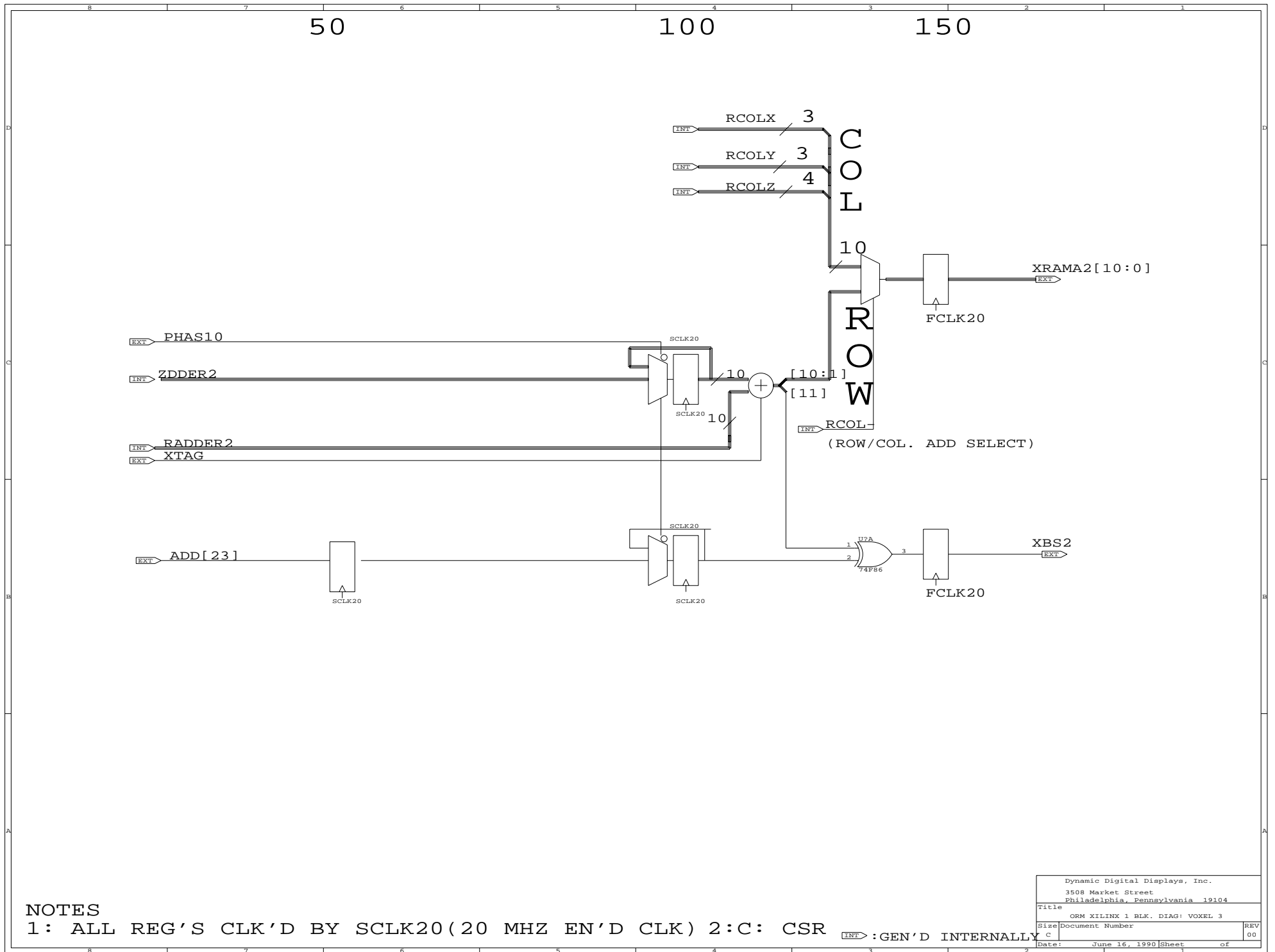
Dynamic Digital Displays, Inc.		
3508 Market Street		
Philadelphia, Pennsylvania 19104		
Title	ORM XILINX0 BLK. DIAG: VOXEL 0	
Size	Document Number	REV
c		00
Date:	June 16, 1990	Sheet of

2:C: CSR :GEN'D INTERNALLY









**NOTES**

1: ALL REG'S CLK'D BY SCLK20(20 MHZ EN'D CLK) 2:C: CSR

INT: GEN'D INTERNALLY

Dynamic Digital Displays, Inc.	
3508 Market Street	
Philadelphia, Pennsylvania 19104	
Title	ORM XILINK 1 BLK. DIAG: VOXEL 3
Size	Document Number
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Date:	June 16, 1990 Sheet 1 of 1